IN THE CLAIMS:

Claims 1-31, 35, 37, 40-43, 47-49 and 52-55 were previously canceled. Claims 32-34, 36, and 44-46 have been amended herein. All of the pending claims 1 through 55 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1-31. (canceled)

32. (currently amended) A method for forming a high density multi-chip module, comprising:

providing a plurality of integrated circuit semiconductor dice, each semiconductor die of said plurality having an active surface having a plurality of bond pads thereon;

forming a substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side;

forming a pattern of a plurality of electrical conductors associated with said substrate on each of said first side and second side of said substrate, at least one electrical conductor of said plurality of electrical conductors having a connection terminal adjacent a through-slot of said at least three elongate through-slots for connecting said plurality of bond pads of a semiconductor die of said plurality of semiconductor dice to an input/output connector;

connecting said ~~conductor~~ pattern of a plurality of electrical conductors on said first side and said second side of said substrate with conductive vias through said substrate;

forming an input/output connector on said substrate and connecting said input/output connector to said plurality of electrical conductors, said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said plurality of semiconductor dice;

attaching the active surfaces of a plurality of said plurality of semiconductor dice to the first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots of

said at least three elongate through-slots for access from the second side of said substrate;

attaching the active surface of at least one semiconductor die of said plurality of semiconductor dice to said second side of said substrate, the plurality of bond pads of said at least one semiconductor die aligned with other alternate through-slots of said at least three elongate through-slots for access from the first side of said substrate;

wire-bonding said plurality of bond pads of each attached semiconductor die of said plurality of semiconductor dice to connection terminals adjacent the alternate through-slots; and

inserting a flowable, hardenable glob-top material into each of said through-slots to encapsulate wires therein, such that said glob-top material extends outwardly toward at least one edge of at least one semiconductor dice adjacent said slot, thereby contacting said at least one edge.

33. (currently amended) The method of claim 32, wherein forming the at least three elongate through-slots comprises forming an elongate stepped surface in said at least three elongate through-slots.

34. (currently amended) The method of claim 33, wherein forming ~~a~~ the pattern of the plurality of electrical conductors includes forming conductive connection terminals on said elongate stepped surface.

35. (canceled)

36. (currently amended) The method of claim 32, wherein a hardenable polymeric material is inserted into each said ~~through-slot.~~at least three elongate through-slots.

37. (canceled)

38. (previously presented) The method of claim 32, further comprising:
performing electrical testing of said plurality of semiconductor dice following wire-bonding thereof and prior to wire encapsulation.

39. (previously presented) The method of claim 32, further comprising:
encapsulating said plurality of dice with a polymeric sealant.

40-43. (canceled)

44. (Currently Amended) A method for forming a high density multi-chip module, comprising:
providing a plurality of integrated circuit dice, each die of said plurality having an active surface with a row of conductive bond pads thereon;
forming a planar substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side;
forming a pattern of electrical conductors associated with said substrate on each of said first and second sides of said substrate and having connection terminals adjacent each of said at least three through-slots for connecting said conductive bond pads to an input/output connector;
connecting said electrical conductor ~~patterns~~ pattern on said first and second sides with conductive vias through said substrate;
forming an input/output connector on said substrate and connecting said input/output connector to said electrical conductors from said conductive bond pads, said forming an input/output connector comprising forming a ball-grid-array on one of said first and second sides of said substrate in a peripheral area surrounding said dice;
attaching the active surfaces of a plurality of said plurality of integrated circuit dice to said first side of said substrate wherein the conductive bond pads thereof are aligned with alternate

through-slots of said at least three through-slots for access from the second side of said substrate;

attaching the active surface of at least one of said plurality of dice to said second side of said substrate wherein the conductive bond pads thereof are aligned with other alternate through-slots for access from the first side of said substrate;

wire-bonding said conductive bond pads of each attached die to connection terminals adjacent the corresponding through-slot; and

inserting a flowable, hardenable glob-top material into each of said at least three elongate through-slots to encapsulate wires therein, such that said glob-top material extends outwardly toward at least one edge of at least one semiconductor dice adjacent said ~~slot,~~ at least three elongate through-slots, thereby contacting said at least one edge.

45. (currently amended) The method of claim 44, wherein forming the at least three elongate through-slots comprises forming an elongate stepped surface in each said ~~through-slot.~~at least three elongate through-slots.

46. (currently amended) The method of claim 45, wherein forming ~~a~~ the pattern of electrical conductors includes forming conductive connection terminals on said elongate stepped surface.

47. (canceled)

48. (canceled)

49. (canceled)

50. (previously presented) The method of claim 44, further comprising:
performing electrical testing of said dice following wire-bonding thereof and prior to wire encapsulation.

51. (previously presented) The method of claim 44, further comprising:
encapsulating said dice with a polymeric sealant.

52-55. (canceled)